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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,709	12/20/2001	Benjamim Tang	35706.5800/66	3875

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EXAMINER	
NGUYEN, DUNG X	

ART UNIT	PAPER NUMBER
2638	

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/029,709	TANG ET AL.	
	Examiner	Art Unit	
	Dung X Nguyen	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20 - 29* is/are allowed.

6)☒ Claim(s) *1 - 3, 8 - 10, 13, and 14* is/are rejected.

7)☒ Claim(s) *4 - 7, 11, 12, and 15 - 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/4/02, 12/20/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: "U.S Patent Application No. XX/XXX.XXX" as recited in paragraph 0001 of the specification must be fulfilled. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> *A person shall be entitled to a patent unless –*
> *(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.*

3. **Claims 1 - 3, 8 - 10, 13, and 14 are rejected** under 35 U.S.C. 102(e) as anticipated by Graef (US patent # 6,101,329).

Regarding claim 1, Graef discloses (figure 1):

- A write counter (18, 19, 20) coupled to a write clock (24), the write counter having a state corresponding to the write clock (15) (column 2, lines 22 - 35);
- A read counter (21, 22, 23) coupled to a read clock (25), the read counter having a state corresponding to the read clock (16) (column 2, line 36 to column 3, line 25);

- Plurality of FIFO registers (12) configured to receive a write data and output a read data using a write clock (24) and read clock (25) (column 3, lines 23 – 25);
- A comparison module (13) configured to determine a fill level of the FIFO register, the fill level corresponding to a comparison of the write counter state (18, 19, 20) and the read counter (21, 22, 23) state (this limitations are inherently taught because Graef would like to determine the ability of the buffer to accept or transmit data, abstract and column 2, lines 4 - 59).

Regarding claim 2, as followed by the limitations analyzed in claimed 1, Graef further discloses that the write and read clocks are asynchronous (column 5, lines 19 – 48).

Regarding claim 3, as followed by the limitations analyzed in claimed 1, Graef further discloses that the comparision comprises a difference between the write counter and the read counter states (this limitation is inherently taught because Graef would like to determine the ability of the buffer to accept or transmit data, column 3, lines 10 - 18).

Regarding claim 8, as followed by the limitations analyzed in claimed 1, Graef further discloses (figure 1) wherein the comparison module (13) comprising a reset counter and a register (column 4, lines 8 - 27).

Regarding claim 9, as followed by the limitations analyzed in claimed 8, Graef further discloses (figure 1) wherein the write counter is used to reset the reset counter (column 4, lines 8 - 27).

Regarding claim 10, as followed by the limitations analyzed in claimed 8, Graef further discloses (figure 1) wherein the reset counter is clocked by the read clock and the register is clocked by the read counter state (column 4, lines 8 - 27).

Regarding claim 13, Graef (discloses (figure 1):

- Receiving a state (15) of write counters (18, 19, 20) in a comparison module (13), the write counters corresponding to the write clock (15) (column 2, lines 22 – 34);

- Receiving a state (16) of read counters (21, 22, 23) coupled to a read clock (25), the read counters corresponding to the read clock (16) (column 2, line 36 to column 3, line 25);
- Receiving a write data in a plurality of FIFO registers (12) and outputting a read data (11) using the write clock (24) and read clock (25) (column 3, lines 23 – 25);
- Determining, in the comparison module (13), a phase difference between the write state and the read state, wherein the phase difference corresponds to the FIFO level in the FIFO registers ((this limitations are inherently taught because Graef would like to determine the ability of the buffer to accept or transmit data, abstract and column 2, line 4 – 49, and column 3, lines 10 - 18).

Regarding claim 14, as followed by the limitations analyzed in claim 13, the limitations are analyzed in the same manner set forth as claim 2.

Allowable Subject Matter

4. **Claims 4 – 7, 11, 12, and 15 - 19 are objected** to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. **Claims 20 – 29 are allowed.** The following is a statement of reasons for the indication of allowable subject matter:

Regarding to the claimed invention, the prior art of record fails to show or render obvious of a PLL/DLL dual loop data serializer, comprising:

A phase locked loop (PLL) including:

- A phase frequency detector (PFD) receiving a local clock;
- A voltage controlled oscillator (VCO);
- A loop filter coupled to the PFD and to the VCO, the loop filter configured to suppress VCO phase noise;

- A phase shifter coupled to the VCO and configured in a feedback loop with the PFD;
- A FIFO register receiving a parallel data input;
- A delayed locked loop (DLL) having a digital loop filter coupled to the phase shifter of the PLL
- A FIFO fill level indicator in the DLL and receiving an input signal from the FIFO register, the indicator including:
    - A write counter coupled to a write clock, the write counter having a state corresponding to the write clock;
    - A read counter coupled to a read clock, the read counter having a state corresponding to the read clock; and
    - A comparison module configured to determine a fill level of the FIFO register, the fill level corresponding to a comparison of the write counter state and the read counter state; and
    - A PISO serializer receiving an input from the FIFO and outputting a serialized data.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Smith (US patent # 6,449,281 B1) discloses an interface control of communication between a control processor and a digital processor.

Carparian (US patent # 5,450,549) discloses a multi-channel array buffer and switching netwaork.

Nawrocki et al. (US patent # 5,263,057) discloses a method of reducing waiting time jitter.

Aoyama (US patent # 4,823,321) discloses a dual port type semiconductor memory device realizing a high speed read operation

Contact Information

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dung X. Nguyen whose telephone number is (571) 272-3010. The examiner can normally be reached on Monday through Friday from 8:00 AM to 17:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Vanderpuye Kenneth N. can be reached on (571) 272-3078. The fax phone numbers for this group is (571) 273-3021.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2600.

DXN
August 16, 2005

KENNETH VANDERPUYE
PRIMARY EXAMINER